

CHW 261: Logic Design

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Digital Fundamentals

CHAPTER 7 Latches, Flip-Flops and Timers

Latches

- **S-R (Set-Reset) latch**
- **Gated S-R latch**
- **Gated D latch**

Latches

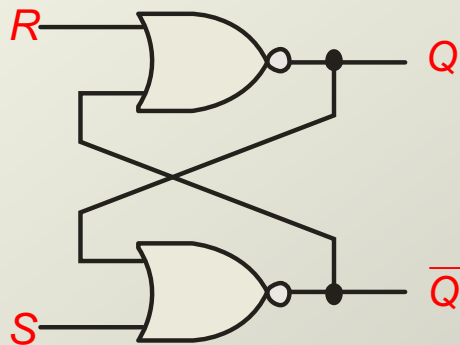
Latches

A **latch** is a **temporary storage device** that has two stable states (bistable). It is a **basic form of memory**.

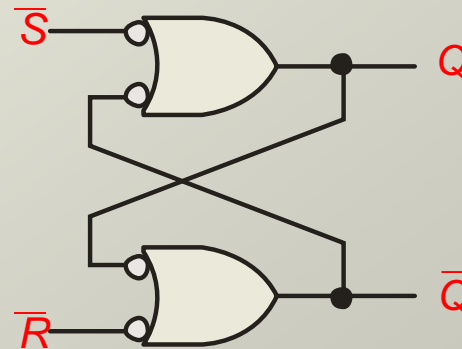
The S-R (Set-Reset) latch is the most basic type. It can be constructed from NOR gates or NAND gates.

With **NOR gates**, the latch responds to **active-HIGH** inputs.

With **NAND gates**, the latch responds to **active-LOW** inputs.



NOR Active-HIGH Latch



NAND Active-LOW Latch

Latches

Active-HIGH S-R Latch

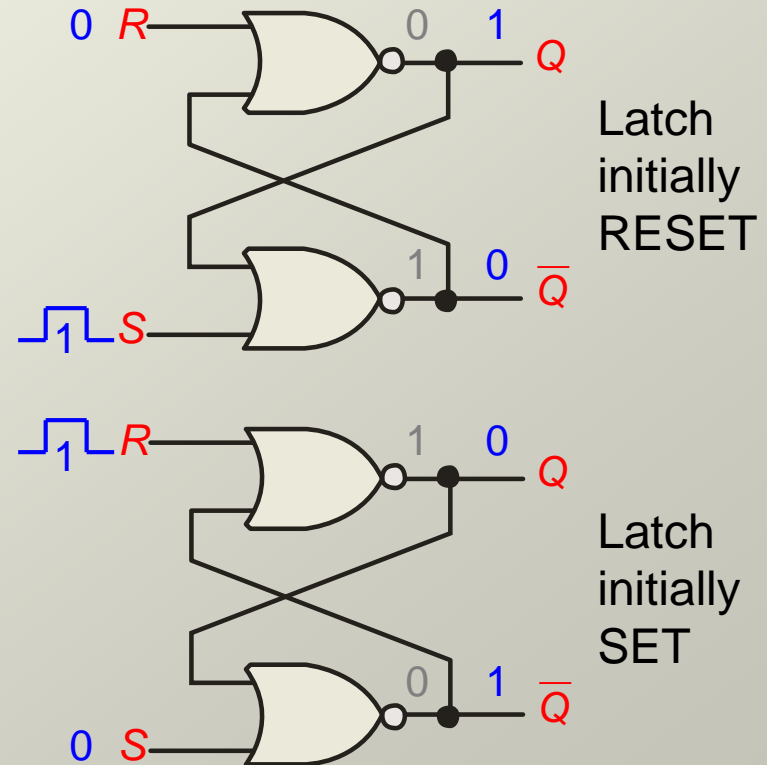
The **active-HIGH** S-R latch is in a stable (latched) condition when both inputs are LOW.

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (0). To SET the latch ($Q = 1$), a momentary HIGH signal is applied to the S input while the R remains LOW.

To RESET the latch ($Q = 0$), a momentary HIGH signal is applied to the R input while the S remains LOW.

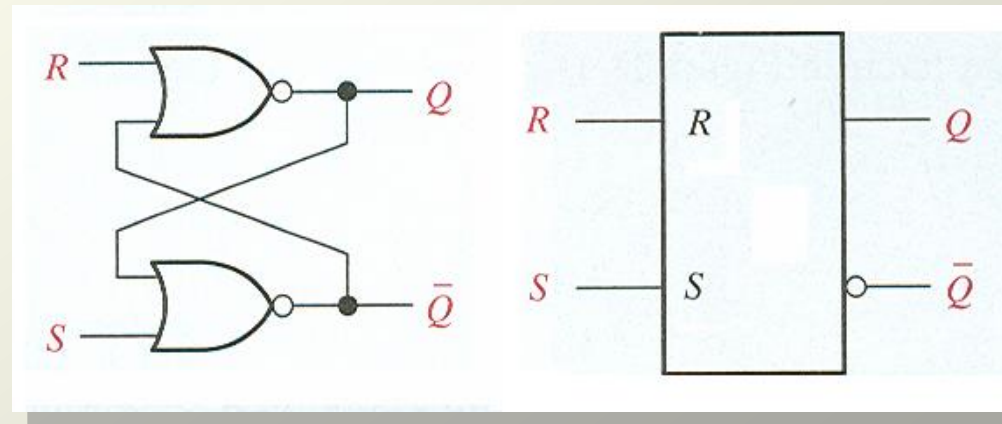
Never apply an active set and reset at the same time (invalid).

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0



Latches

Active-HIGH S-R Latch



INPUTS		OUTPUTS		COMMENTS
S	R	Q	\bar{Q}	
0	0	NC	NC	No change. Latch remains in present state.
0	1	0	1	Latch RESET.
1	0	1	0	Latch SET.
1	1	0	0	Invalid condition

Latches

Active-LOW S-R Latch

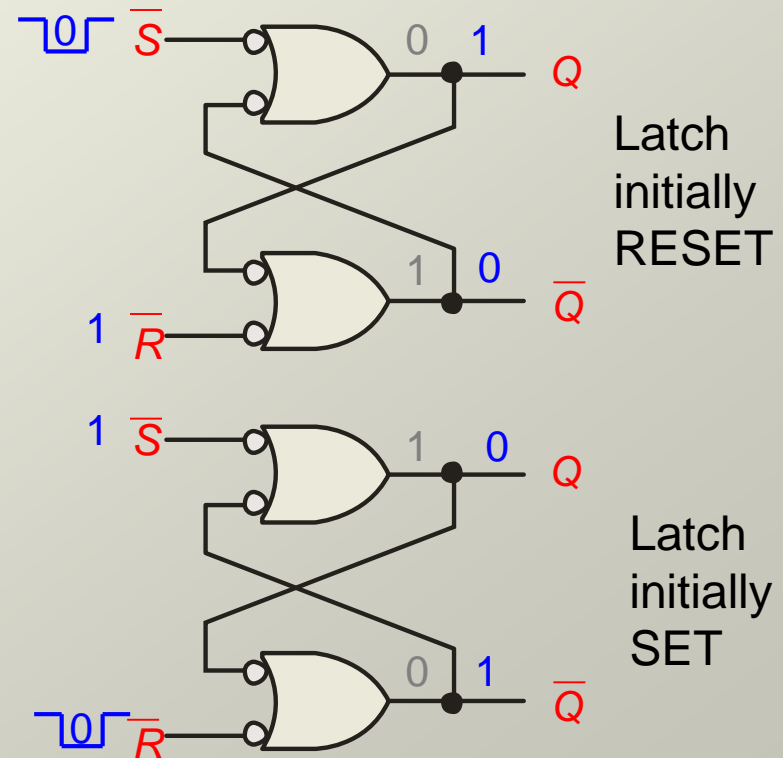
The **active-LOW** \bar{S} - \bar{R} latch is in a stable (latched) condition when both inputs are HIGH.

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (1). To SET the latch ($Q = 1$), a momentary LOW signal is applied to the \bar{S} input while the \bar{R} remains HIGH.

To RESET the latch a momentary LOW is applied to the \bar{R} input while \bar{S} is HIGH.

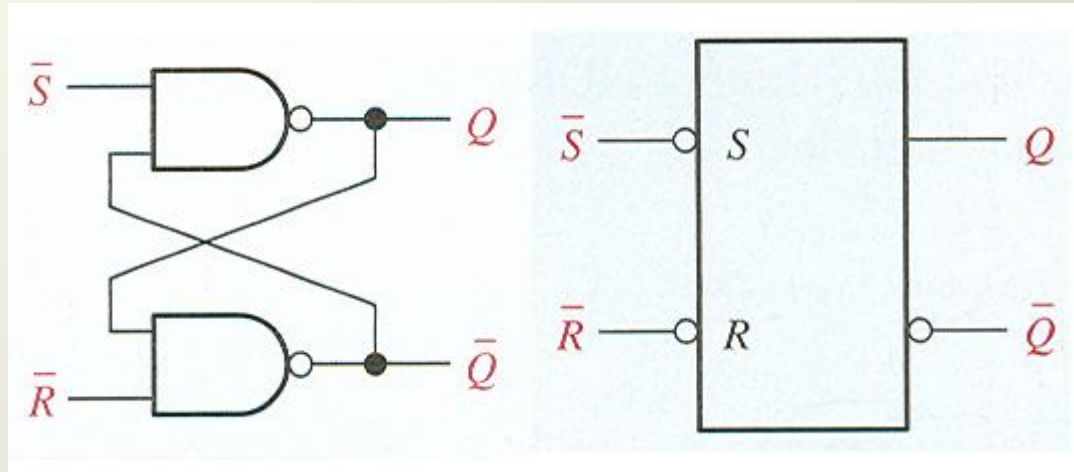
Never apply an active set and reset at the same time (invalid).

Inputs		Output
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0



Latches

Active-LOW S-R Latch



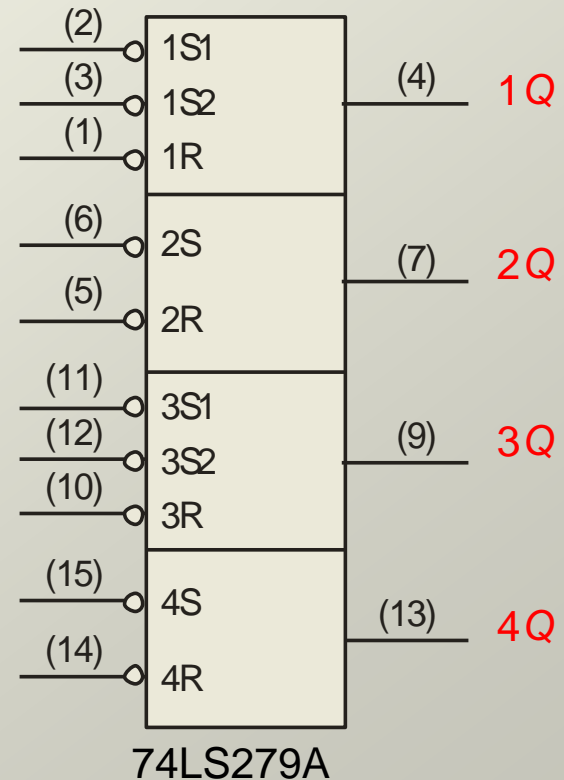
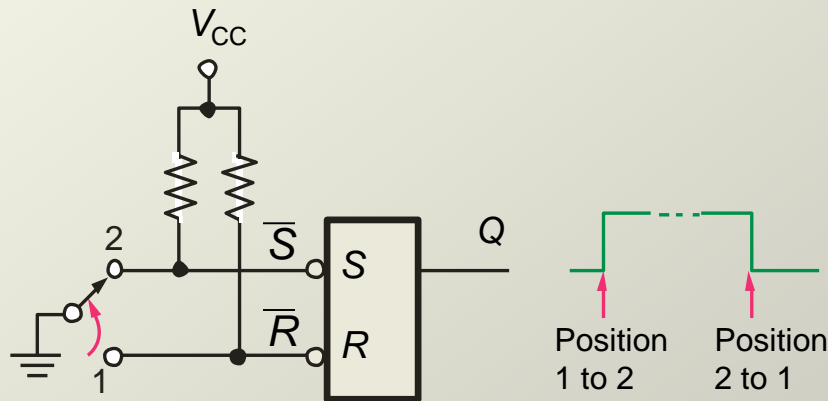
INPUTS		OUTPUTS		COMMENTS
\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

Latches

Latches

The active-LOW \bar{S} - \bar{R} latch is available as the 74LS279A IC.

\bar{S} - \bar{R} latches are frequently used for switch debounce circuits as shown:



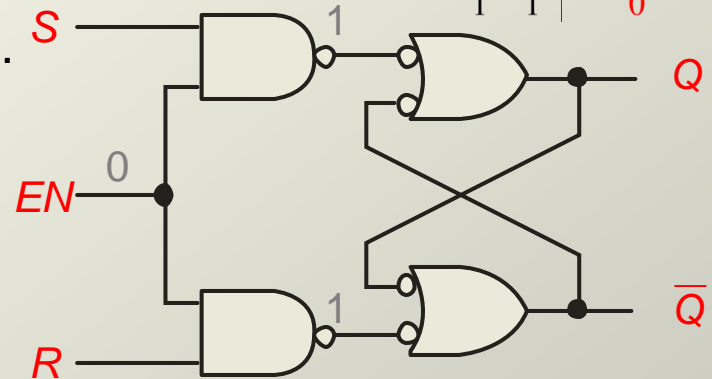
Latches

Latches

A gated latch is a variation on the basic latch.

The gated latch has an additional input, called **enable (EN)** that must be **HIGH** in order for the latch to respond to the S and R inputs.

Inputs		Output
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

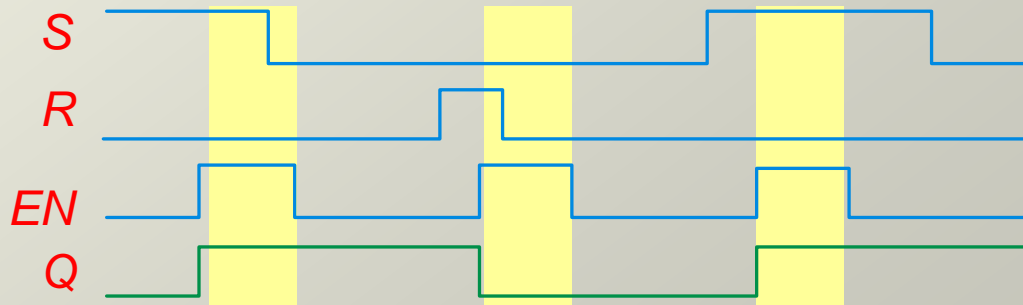


Example

Show the Q output with relation to the input signals. Assume Q starts LOW.

Solution

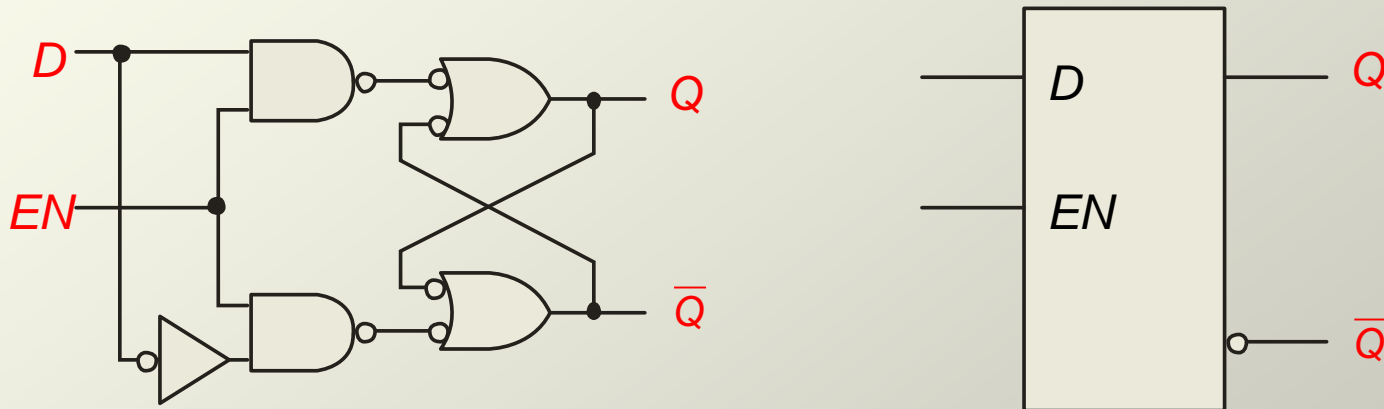
Keep in mind that S and R are only active when EN is HIGH.



Latches

Latches

The D latch is an variation of the S - R latch but combines the S and R inputs into a single D input as shown:



A simple rule for the D latch is:

Q follows D when the Enable is active.

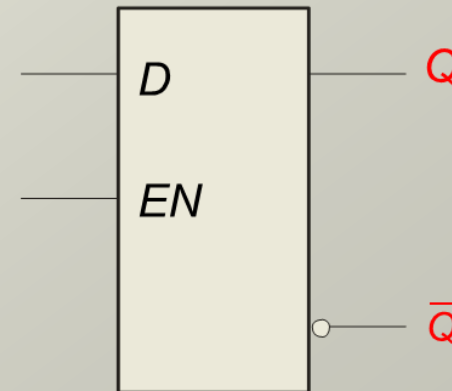
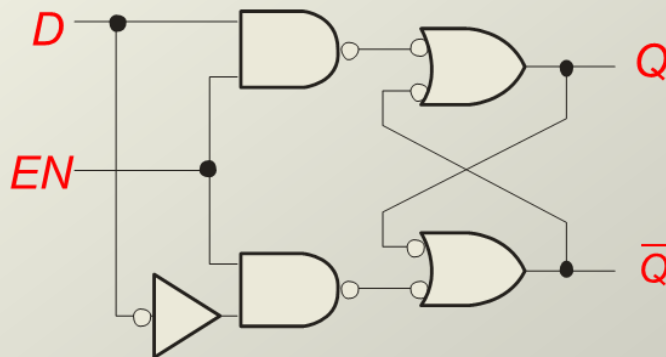
Latches

Latches

The truth table for the D latch summarizes its operation.

If EN is LOW, then there is no change in the output and it is latched.

Inputs		Outputs		Comments
D	EN	Q	\bar{Q}	
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	\bar{Q}_0	No change

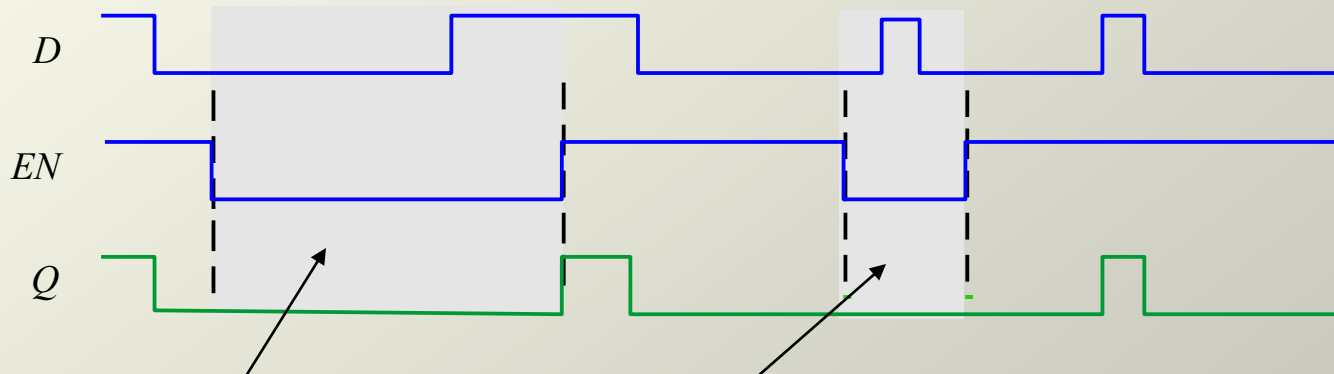
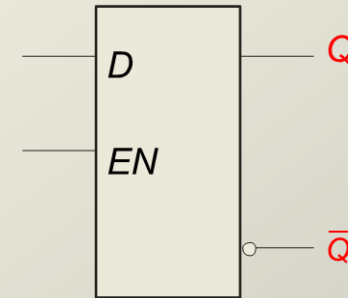


Latches

Latches

Example

Determine the Q output for the D latch, given the inputs shown.



Notice that the Enable is not active during these times, so the output is latched.

Edge-Triggered Flip-Flops

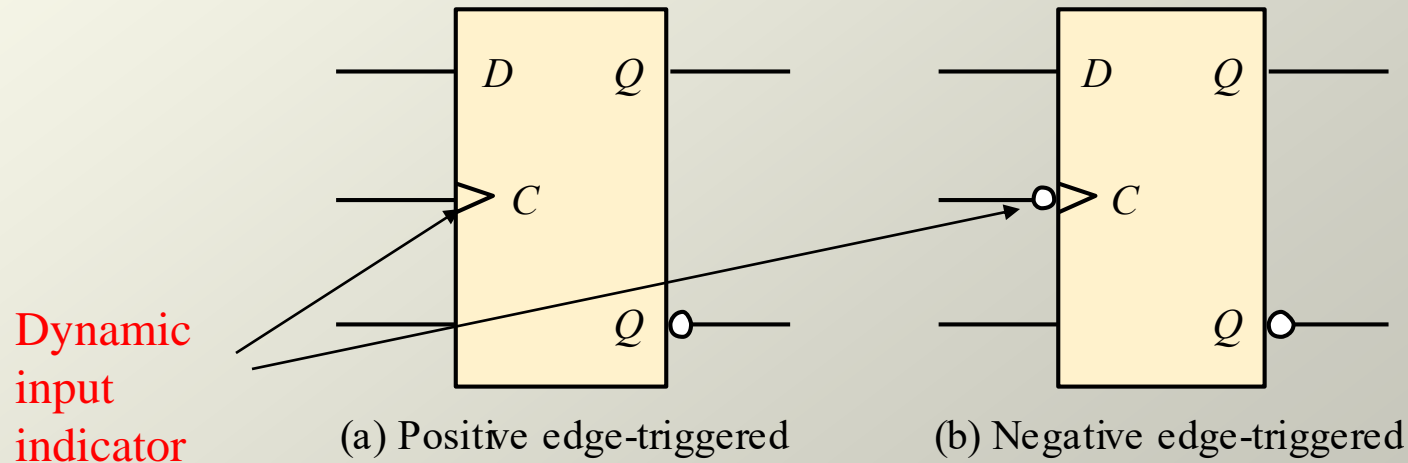
- **Edge-triggered D flip-flop**
- **Edge-triggered J-K flip-flop**

Edge-Triggered Flip-Flops

Flip-flops

A flip-flop differs from a latch in the manner it changes states. **A flip-flop is a clocked device**, in which only the clock edge determines when a new bit is entered.

The active edge can be positive or negative.



Edge-Triggered Flip-Flops

Flip-flops

The truth table for a positive-edge triggered D flip-flop shows an up arrow to remind you **that it is sensitive to its D input only on the rising edge of the clock; otherwise it is latched.** The truth table for a negative-edge triggered D flip-flop is identical except for the direction of the arrow.

Inputs		Outputs		Comments
D	CLK	Q	\bar{Q}	
1	↑	1	0	SET
0	↑	0	1	RESET

(a) Positive-edge triggered

Inputs		Outputs		Comments
D	CLK	Q	\bar{Q}	
1	↓	1	0	SET
0	↓	0	1	RESET

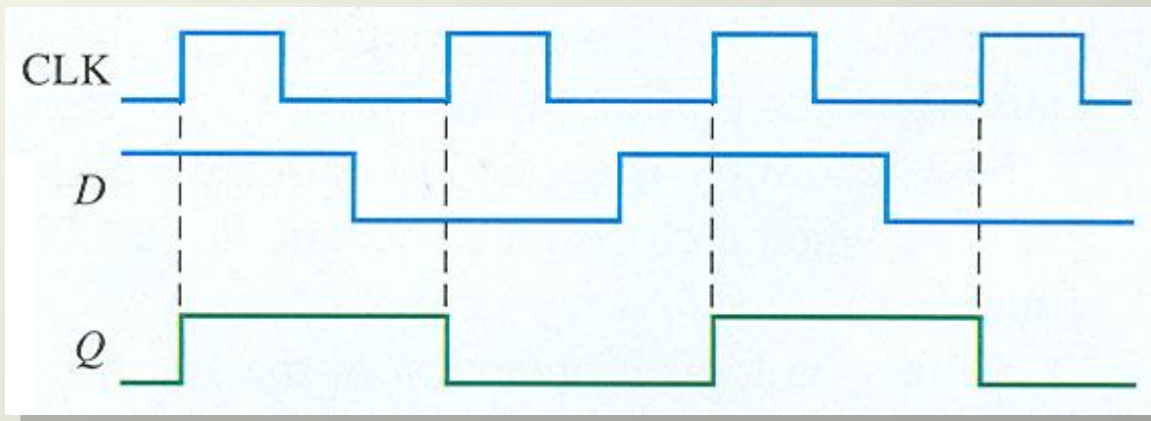
(b) Negative-edge triggered

Edge-Triggered Flip-Flops

Edge-triggered D flip-flop

INPUTS		OUTPUTS		COMMENTS
D	CLK	Q	\bar{Q}	
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH



Edge-Triggered Flip-Flops

Flip-flops

The J-K flip-flop is more versatile than the D flip flop.

In addition to the clock input, **it has two inputs**, labeled J and K . When both J and $K = 1$, the output changes states (**toggles**) on the active clock edge (in this case, the rising edge).

Inputs			Outputs		Comments
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	\bar{Q}_0	Q_0	Toggle

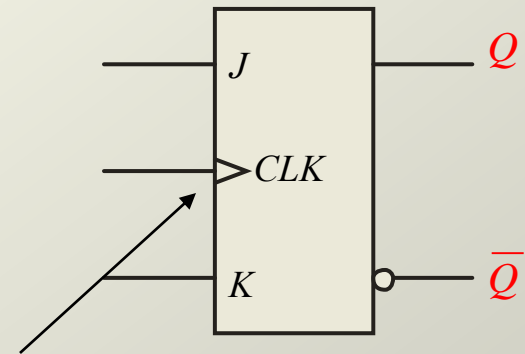
Edge-Triggered Flip-Flops

Edge-triggered J-K flip-flop

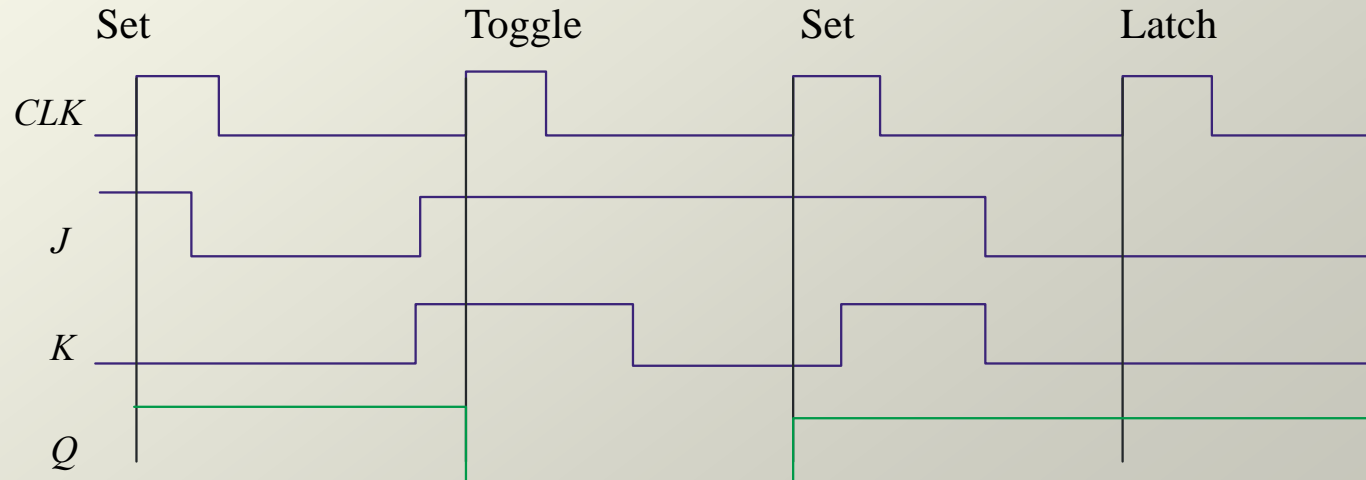
Example

Determine the Q output for the J - K flip-flop, given the inputs shown.

Notice that the outputs change on the leading edge of the clock.



Solution



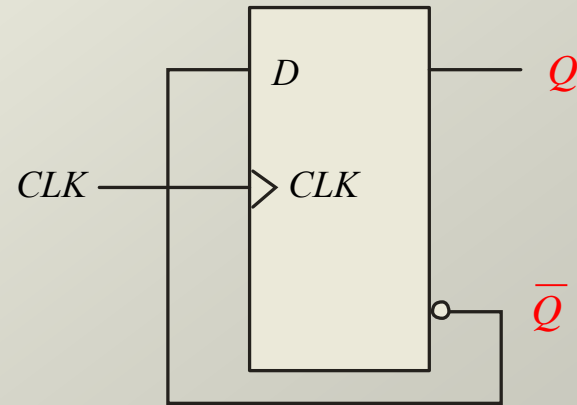
Edge-Triggered Flip-Flops

Flip-flops

A D-flip-flop does not have a toggle mode like the J-K flip-flop, but you can hardwire a toggle mode by connecting \bar{Q} back to D as shown. This is useful in some counters as you will see in Chapter 8.

For example, if Q is LOW, \bar{Q} is HIGH and the flip-flop will toggle on the next clock edge. Because the flip-flop only changes on the active edge, the output will only change once for each clock pulse.

Inputs		Outputs		Comments
D	CLK	Q	\bar{Q}	
1	↑	1	0	SET
0	↑	0	1	RESET



D flip-flop hardwired for a toggle mode

Edge-Triggered Flip-Flops

Flip-flop Applications

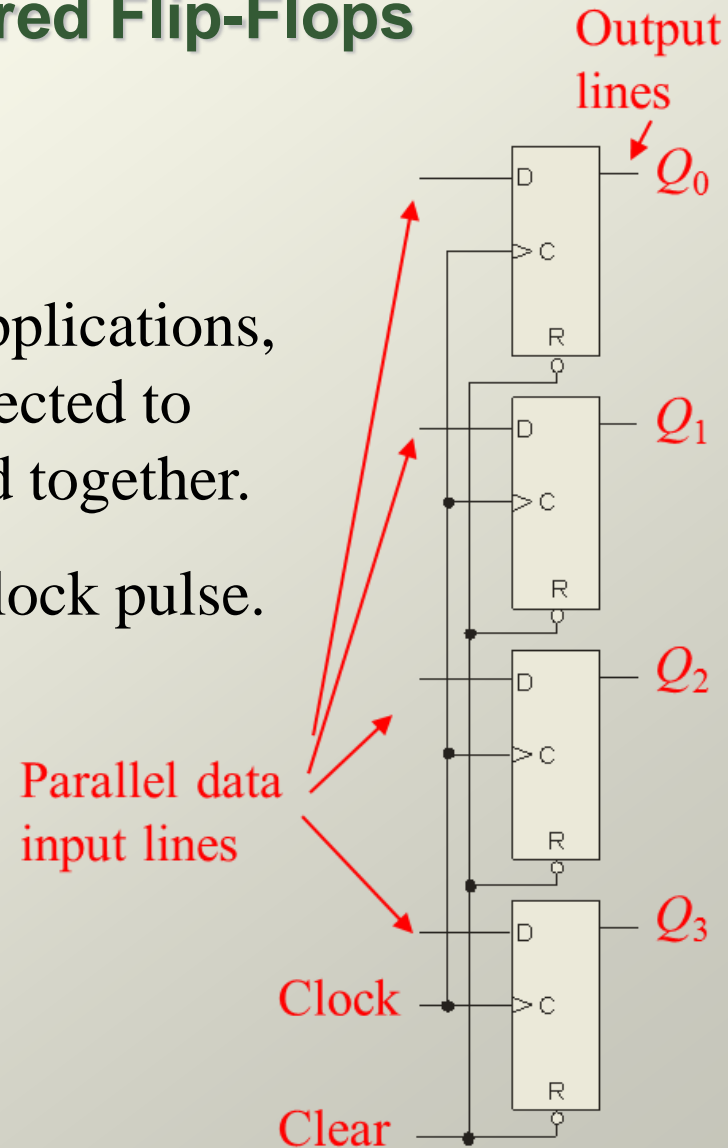
Principal flip-flop applications are for temporary **data storage**, as **frequency dividers**, and in **Counters** (which are covered in detail in Chapter 8).

Edge-Triggered Flip-Flops

Flip-flop Applications

Typically, for **data storage** applications, a group of flip-flops are connected to parallel data lines and clocked together.

Data is stored until the next clock pulse.



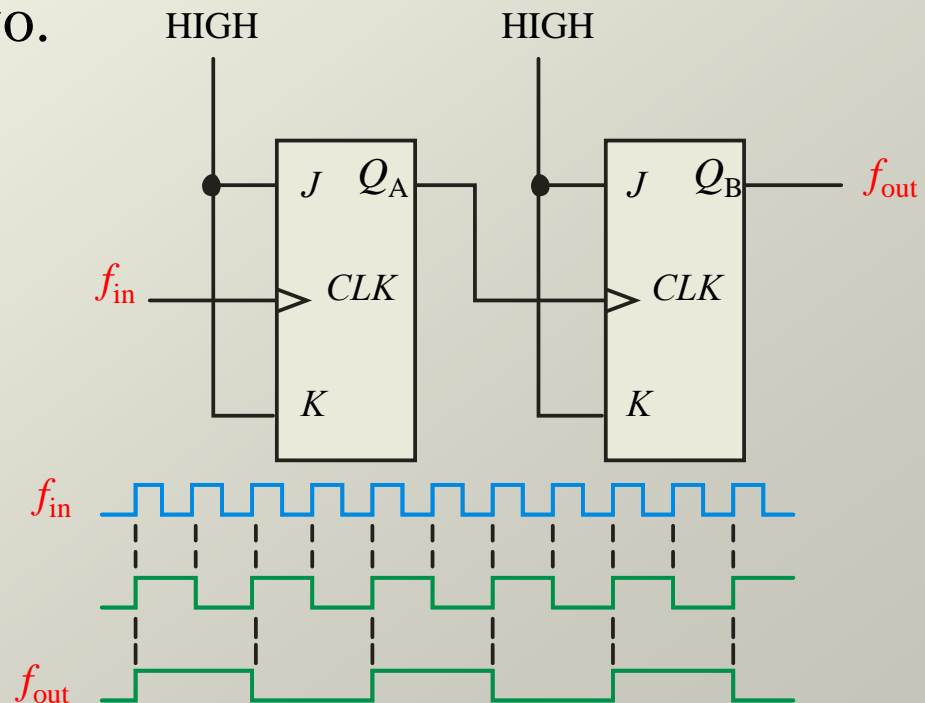
Edge-Triggered Flip-Flops

Flip-flop Applications

For **frequency division**, it is simple to use a flip-flop in the toggle mode or to chain a series of toggle flip flops to continue to divide by two.

One flip-flop will divide f_{in} by 2, two flip-flops will divide f_{in} by 4 (and so on). A side benefit of frequency division is that the output has an exact 50% duty cycle.

Waveforms:



Multivibrator

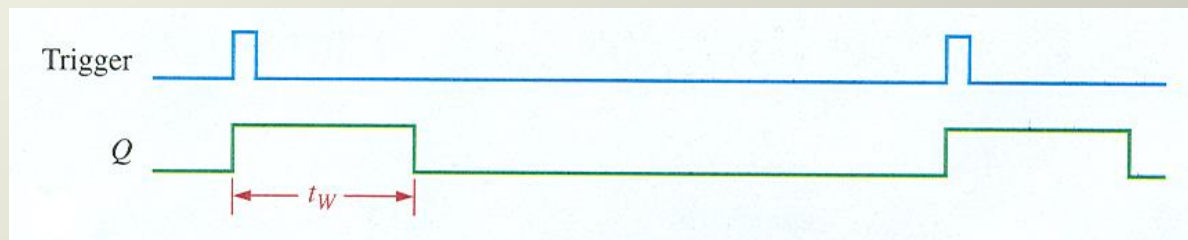
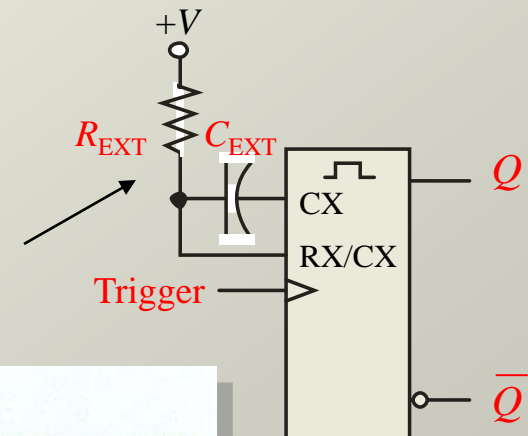
- **Monostable (One-Shot)**
- **Astable.**

Multivibrator

Monostable

The **monostable** or **one-shot** multivibrator is a device with **only one stable state**. When triggered, it goes to its unstable state for a predetermined length of time, then returns to its stable state.

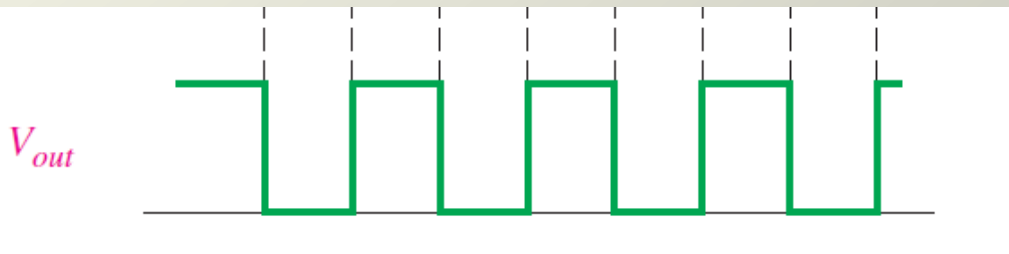
For most one-shots, the **length of time in the unstable state (t_W) is determined by an external RC circuit.**



Multivibrator

Astable

An **astable** multivibrator is a device that has **no stable states**; it changes back and forth (oscillates) between two unstable states without any external triggering. The resulting output is typically **a square wave that is used as a clock signal** in many types of sequential logic circuits.

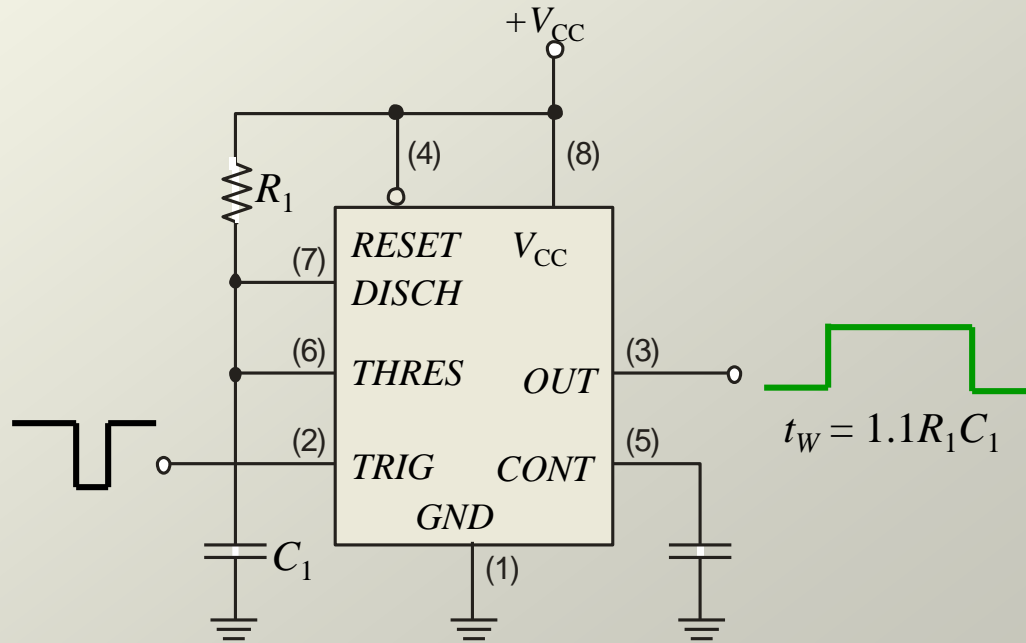


Multivibrator

The 555 timer

The 555 timer can be **configured in various ways**. A basic **monostable** is shown. The pulse width is determined by $R_1 C_1$ and is approximately $t_W = 1.1R_1 C_1$.

The trigger is a negative-going pulse.



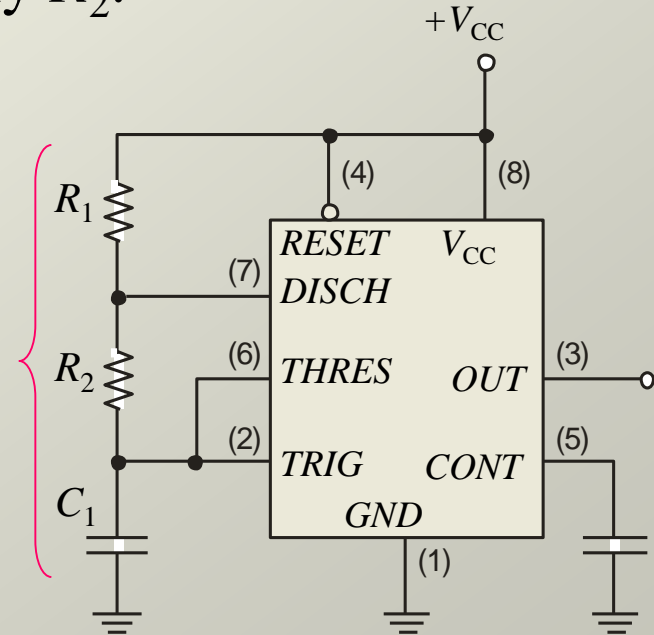
Multivibrator

The 555 timer

The 555 can be configured as a basic **astable multivibrator** with the circuit shown. In this circuit C_1 charges through R_1 and R_2 and discharges through only R_2 .

The output frequency is given by:

$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$



Multivibrator

The 555 timer

Given the components, you can read the frequency from the chart. Alternatively, you can use the chart to pick components for a desired frequency.

